Beyond Chip Stacking---Quilt Packaging Enabled 3D Systems

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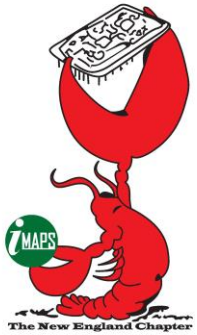

2016 New England IMAPS Symposium

Indiana Integrated Circuits LLC

Presentation Overview

1. Introduction to Indiana Integrated Circuits
2. Introduction to Quilt Packaging interconnect technology & fabrication description
3. Brief overview of QP electrical & mechanical performance & reliability
4. 3D Systems enabled using Quilt Packaging
5. Summary/Discussion

Indiana Integrated Circuits, LLC (IIC)

Formed to commercialize Quilt Packaging (QP) – a ground breaking packaging technology invented at Notre Dame.

- Founded by Kulick & Bernstein (2009)
- Main office South Bend, IN at Innovation Park (also CO & NC)
- IIC has experienced steady growth with customers & partners across multiple industry sectors since early in it's inception.
- Operations funded directly through revenue growth and through equity investment (Series A closed late 2015).
- The QP process is commercially available at RTI International.
- Process development for medium volume requirements is ongoing at Rogue Valley Microdevices in Medford, OR.

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IIC Business Model--Licensing
(supported by prototyping)

…and more proprietary.

- IIC works with customers to integrate QP into their systems.
- First-adopters have been aerospace/defense applications.
- QP is platform technology (3D, microwave, power, optical, biomed, more)
- Expansion beyond DOD to commercial underway

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Existing Supply Chain—Wafer Processing

- RTI International, Inc.
  - ITAR compliant BEOL facility located in Durham/RTP, NC
  - Wafer post-processing for deep etch, plating, CMP, singulation
  - Si & SiC substrates from pieces up o 8” wafers
  - IIC partner since 2012
  - Offering QP MPW service
  - Can support up to 100 wafer starts per month

- Rogue Valley Microdevices, Inc.
  - Pure-play MEMS foundry located in Medford, OR
  - Wafer post-processing for thin film, etching, litho (deep etch coming)
  - Multiple substrates, up to 8” wafers
  - IIC partner since January 2015 (MIG Tech. Pitch win award)
  - Can support several hundred wafer starts per month

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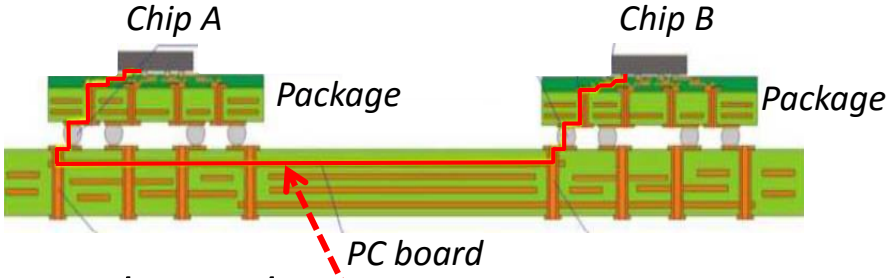
Existing Supply Chain—Assembly

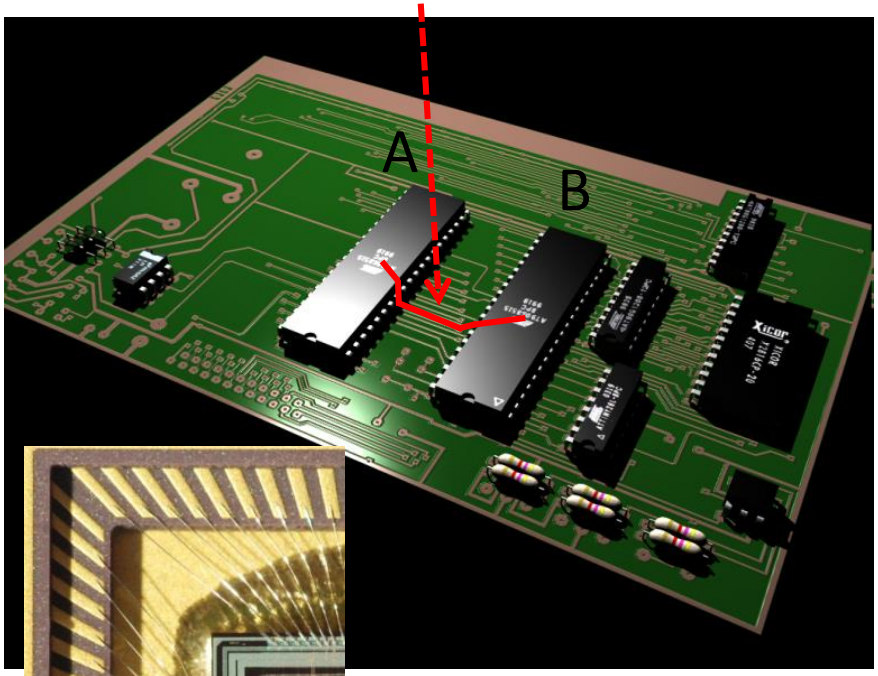
- Automated Tooling: MRSI Systems, Inc.
  - Global supplier of fully-automated solutions for assembly of microelectronic devices
  - High precision die attach & dispensing systems
  - Demonstrated automated Quilt Package assembly on MRSI 705 system
  - Working with since 2012
  - Based in Billerica, MA

- North American-based Low to Medium Volume Assembler
  - Public announcement coming soon (Spring 2016)
  - Leader in electronics design, manufacturing and aftermarket services
  - Can support DOD applications

Existing Microchip Packaging



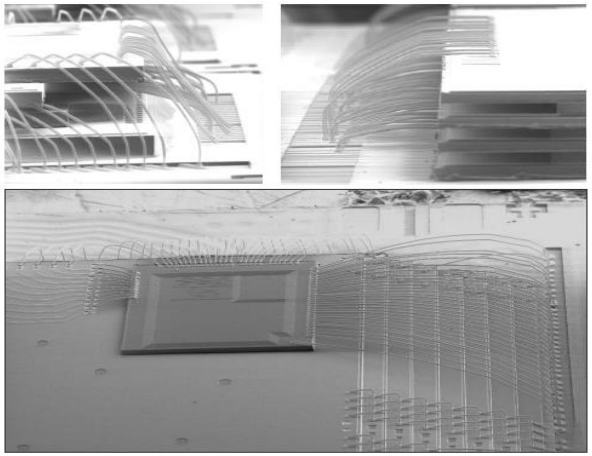
Electrical Signal



"…Overall performance, cost, size and functionality of a system will be limited by….the off-chip interconnects."

-International Technology Roadmap For Semiconductors

Existing technologies waste:



- Power
- Time
- Money
- Space

Packaging has become a system constraint.

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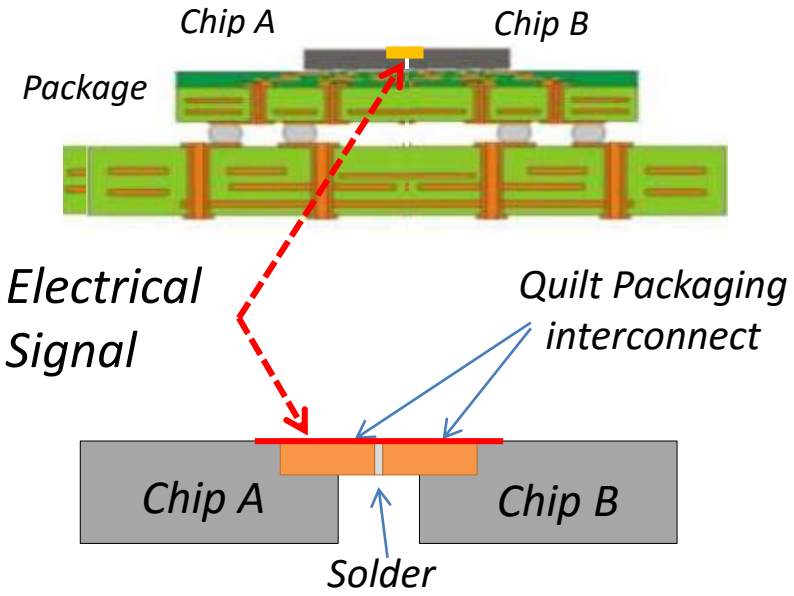
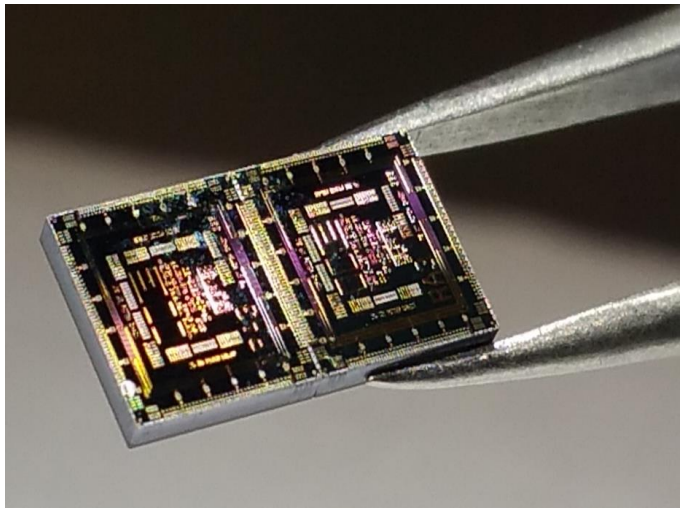
Quilt Packaging Interconnect Technology





Quilt Packaging is a patented, ***direct*** edge-to-edge chip interconnect technology that can be implemented in disparate materials and technologies (Si, GaAs, InP, GaN/SiC, SiGe, GaSb,etc.)

Quilt Packaging enables 10x to 100X improvement.

- Power--- 10x lower parasitic losses
- Time---10x faster
- Money---Order of magnitude total system cost savings
- Space---Dramatic form factor reduction

Quilt Packaging enables new system designs

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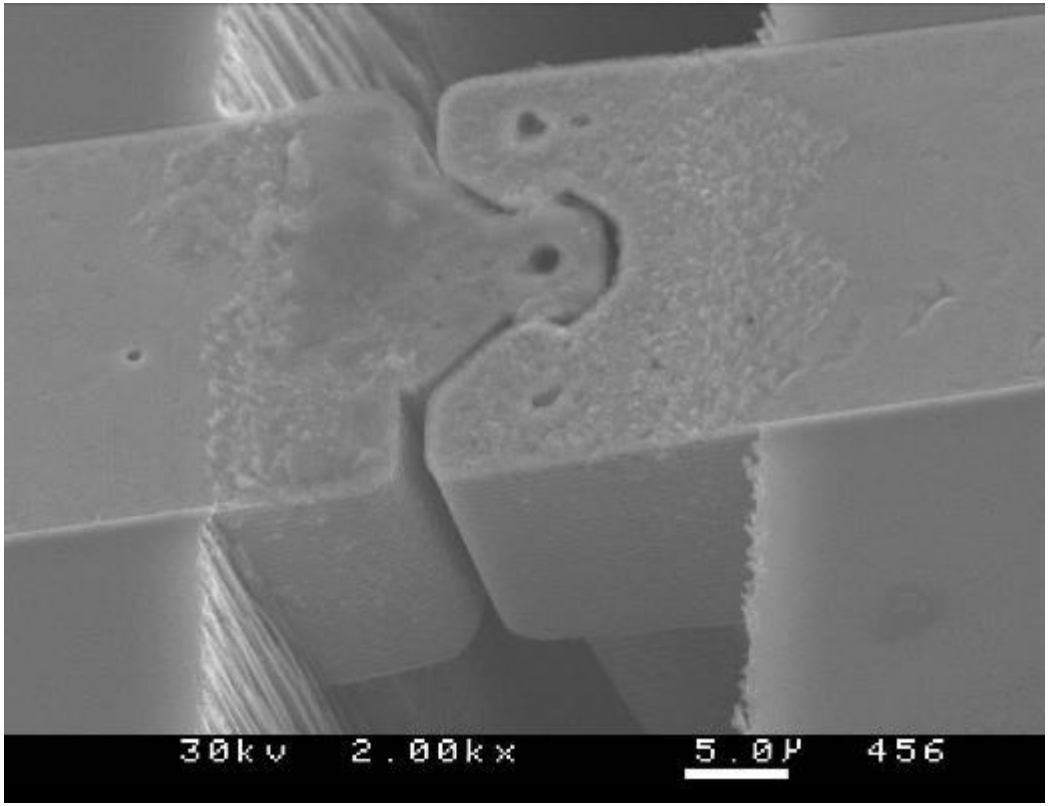
QP-Interconnect Structures

- Edge connection structures called “nodules”
- Solid metal, typically Cu, 5-500 um wide, 20-50 um thick
- 10 um pitch possible
- Customizable shapes- including interlocking- *enables sub-micron chip alignment*



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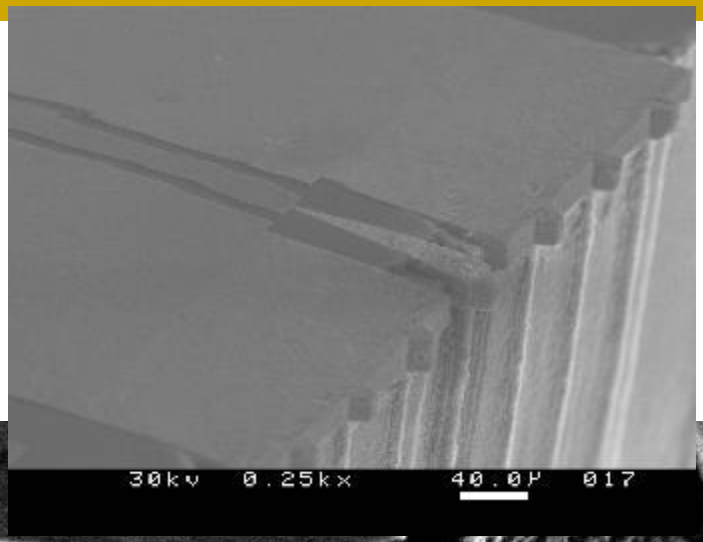
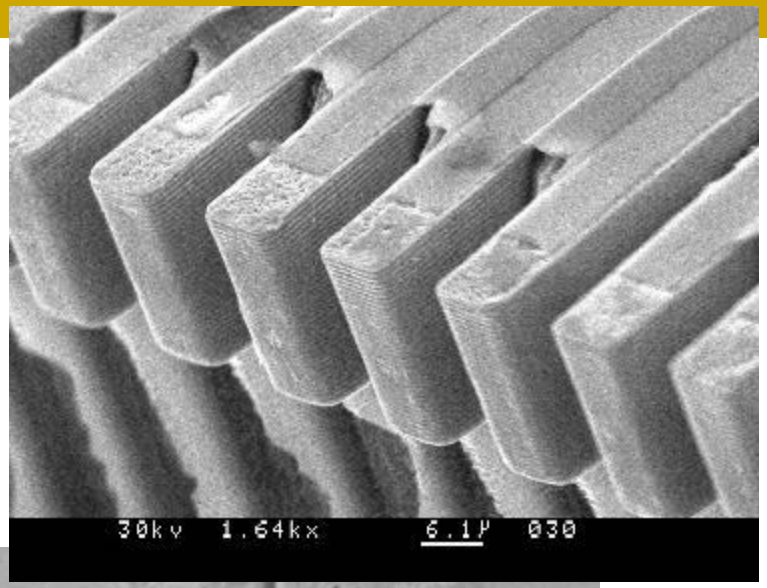
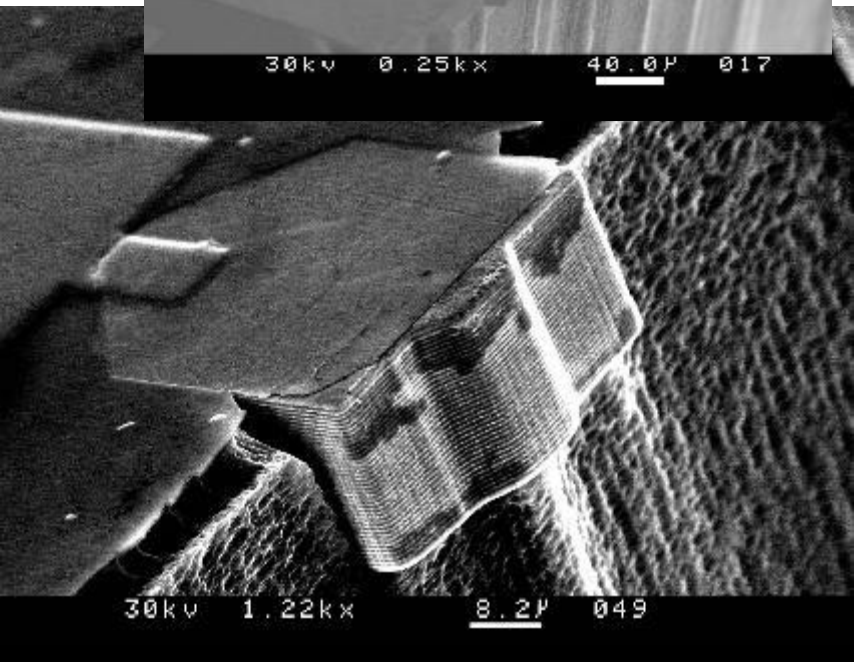
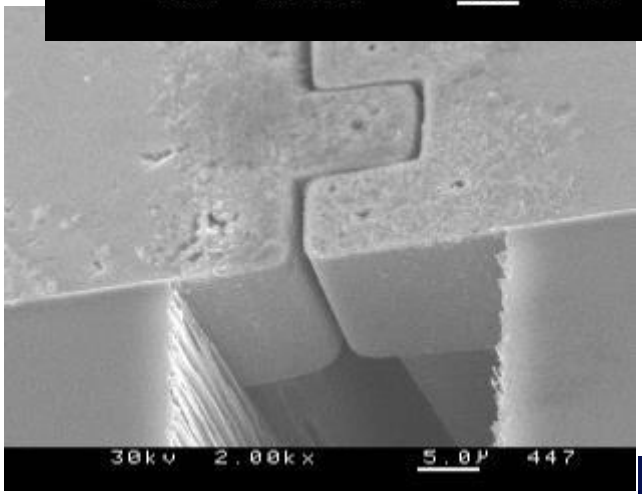
QP Customizable I/O









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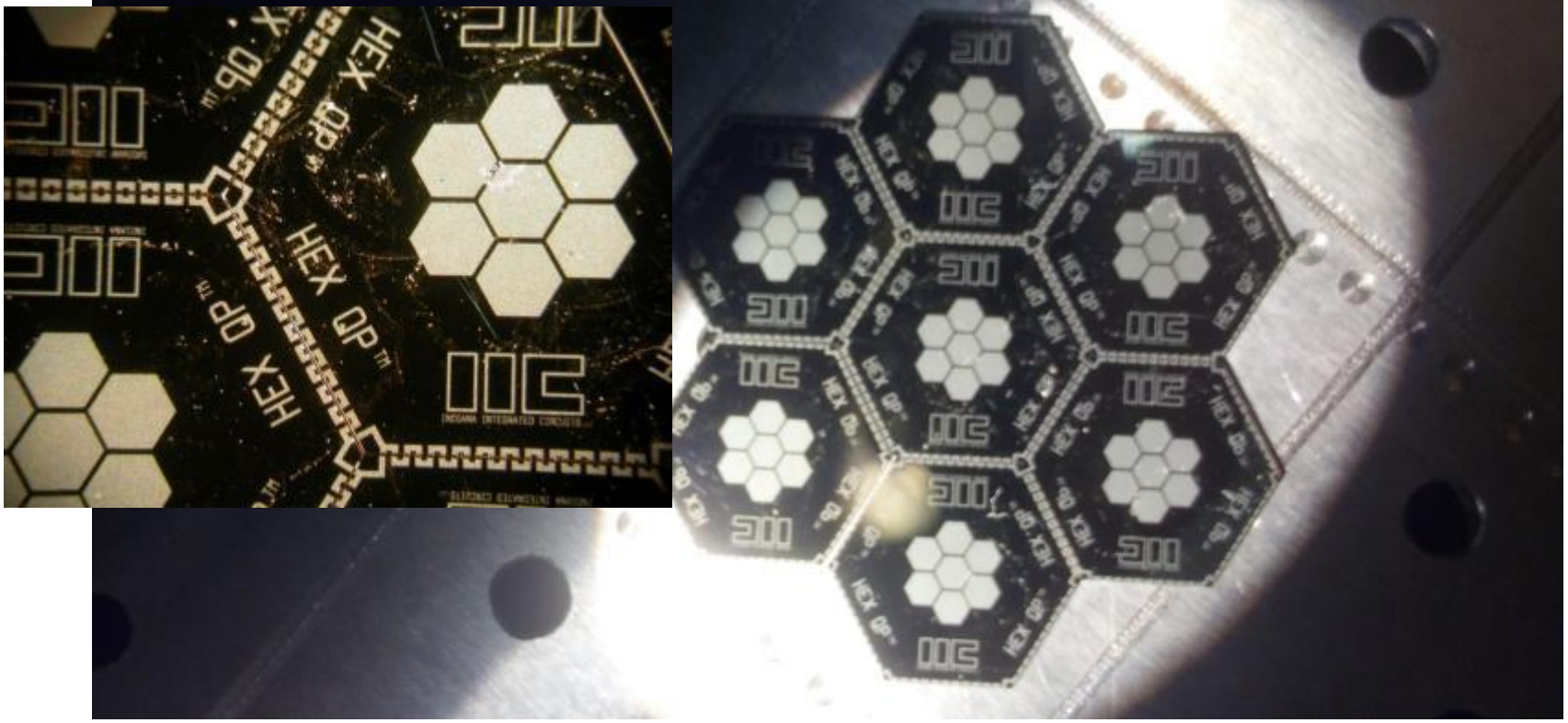
QP Supports Customized Geometries example - HexQP™



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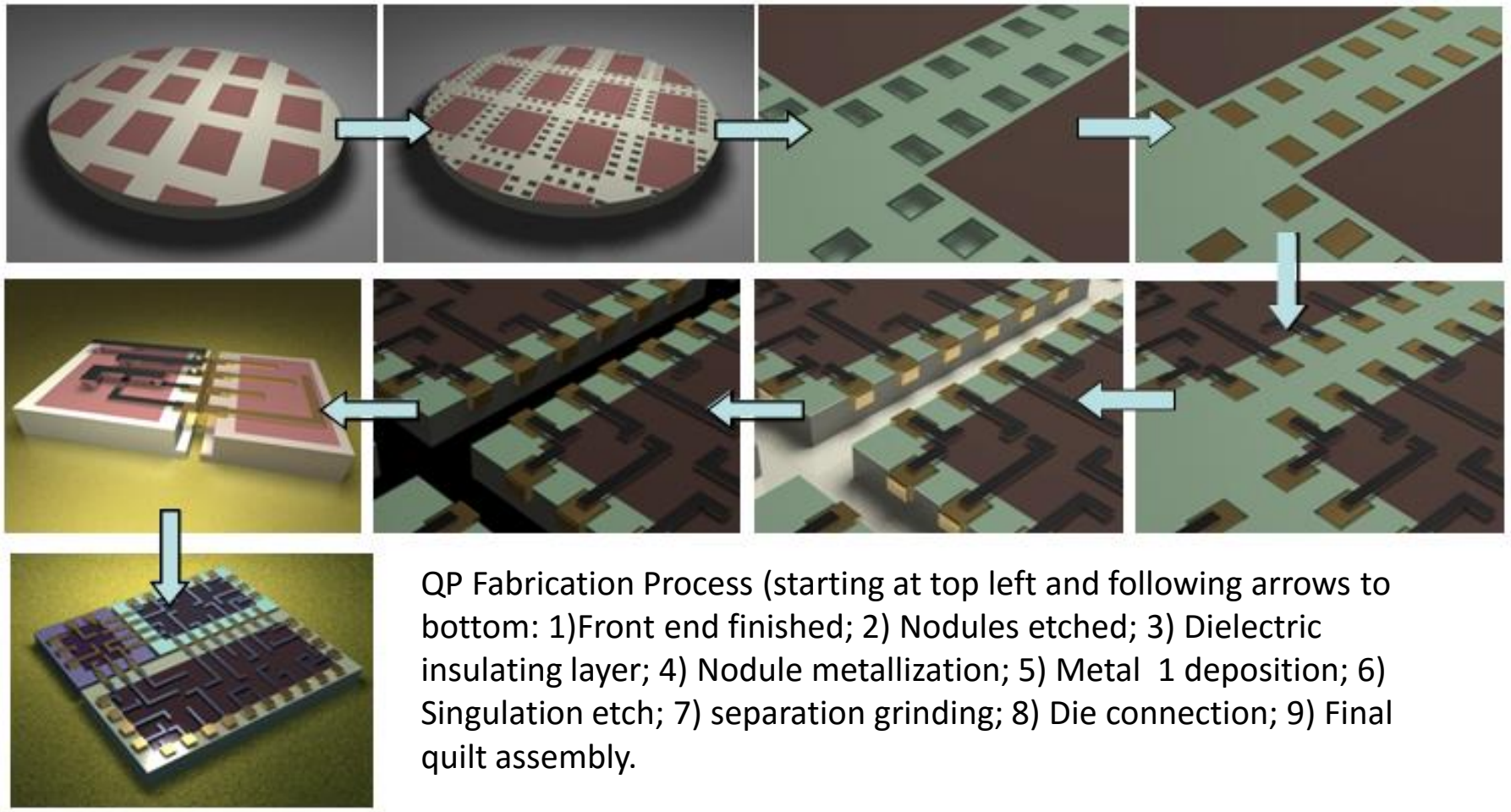
Quilt Packaging Process Overview



QP Fabrication Process (starting at top left and following arrows to bottom: 1)Front end finished; 2) Nodules etched; 3) Dielectric insulating layer; 4) Nodule metallization; 5) Metal 1 deposition; 6) Singulation etch; 7) separation grinding; 8) Die connection; 9) Final quilt assembly.

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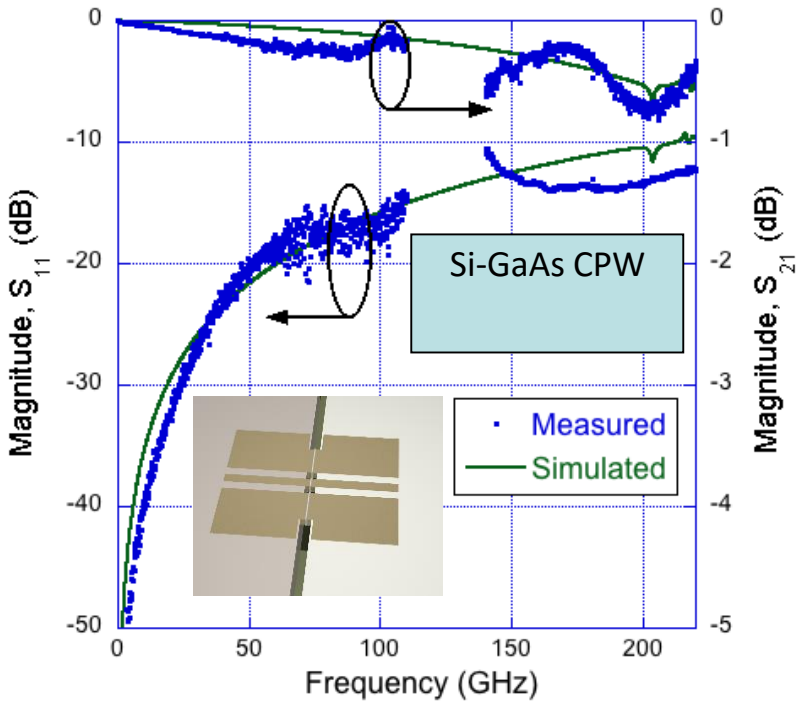
Quilt Packaging Electrical Performance
(Performs as if it were an *on-chip* interconnect)

- Homogeneous (e.g. Si-Si, GaAs-GaAs) and heterogeneous (Si-GaAs, Si-InP, etc.) interconnects demonstrated
- Excellent RF/millimeter-wave, high speed digital performance:
  - Less than 0.1 dB S_{21} from DC-100 GHz
  - $S_{21} \leq 0.75$ dB to 220 GHz
  - 43 Gb/s eyes with no impairment
- Ultra-low parasitics
- Dense I/O pitch at chip edge (10 um pitch)
- Extremely high current-handling capacity > 10 **A t**hrough 30 µm x 20 µm nodules without damage



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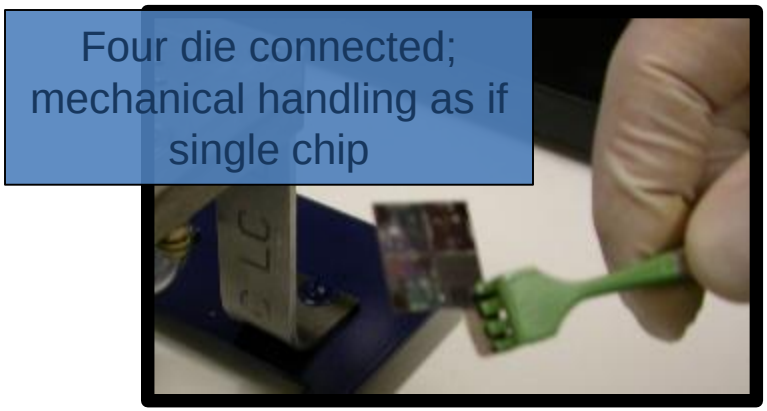
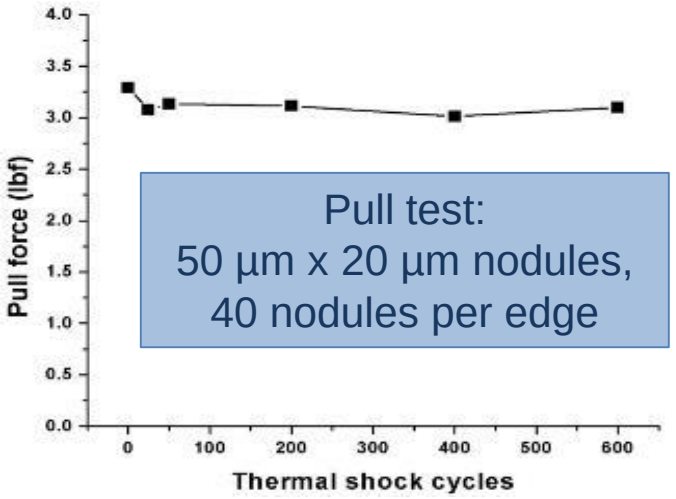
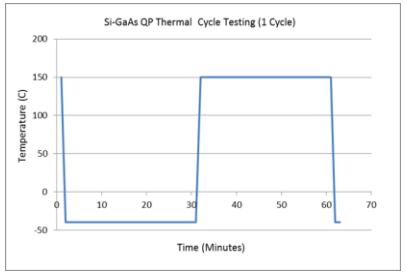
Quilt Packaging: Mechanical Performance

- Extremely robust mechanically
- Interconnected “quilt” can often be handled like larger chip (e.g. pick & place, etc.)
- Thermal test -40 C to 125 C, 1000+ cycles, no failures
- Tested to 77K from ambient, no failures for mounted or un-mounted
- Pull testing requires large force before failure







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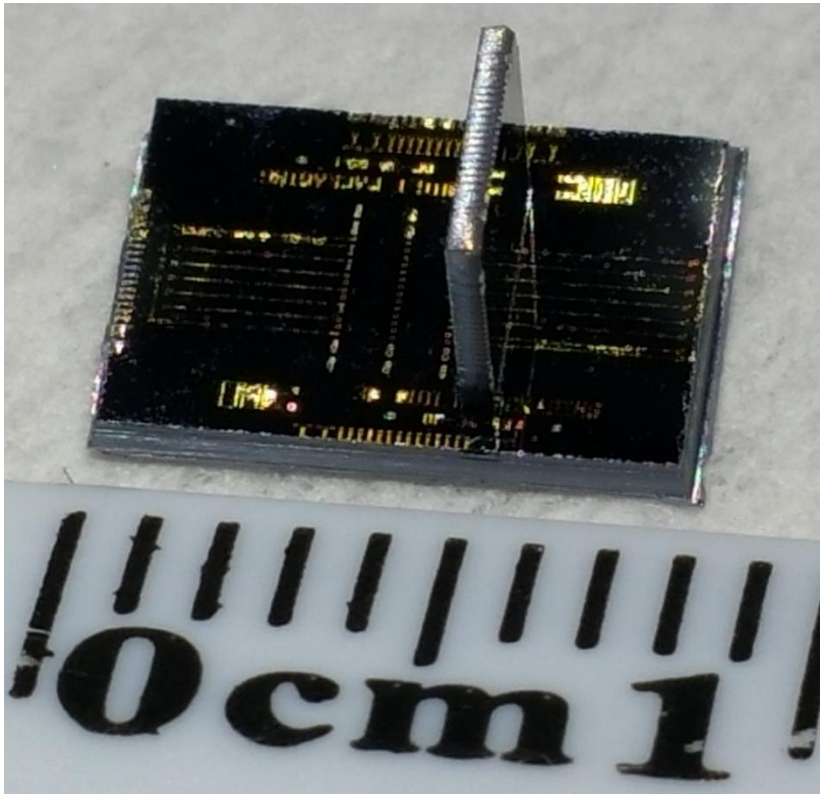
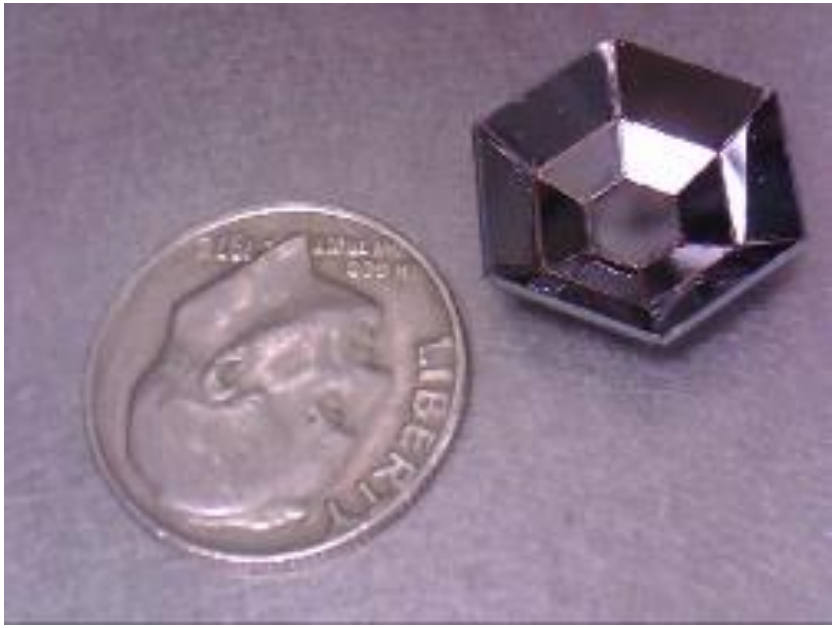
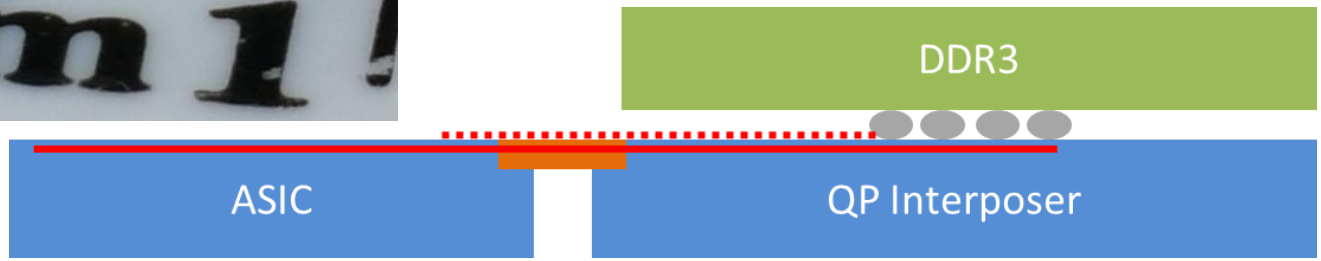
“3DQP” Variations: Orthogonal, Alternative Geometry, Stacked QP







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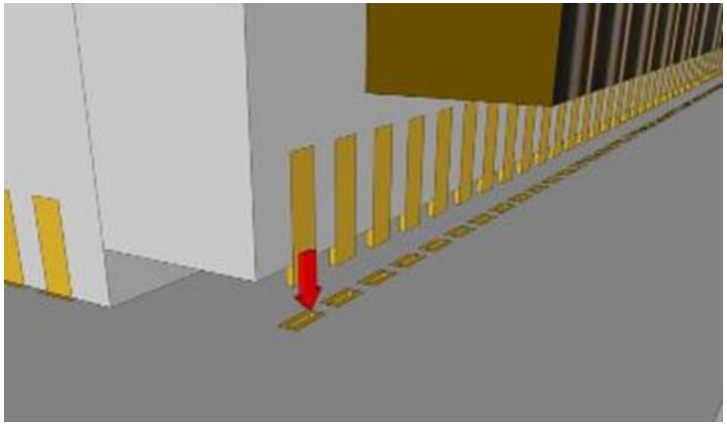
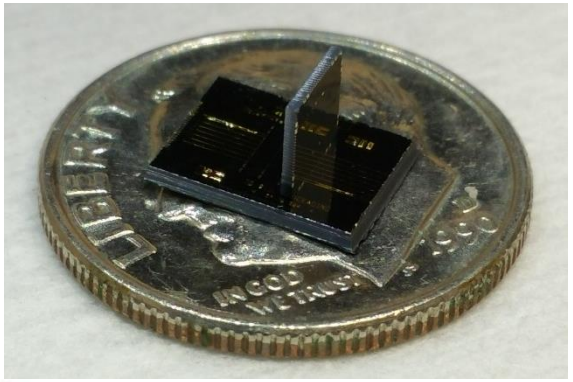
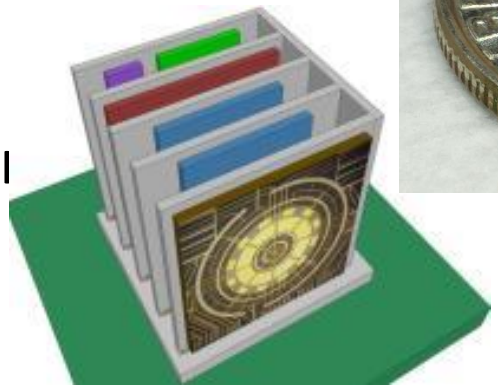
3DQP---Orthogonal Integration

- “Daughter Card” into “Motherboard” approach
- Utilizes standard QP chip for vertical or “daughter card” elements
- QP interconnect nodules plug into a socket on MB
- Applications include system miniaturization, IMU, power electronics & VCSEL integratio
- Technology demonstration currently underway







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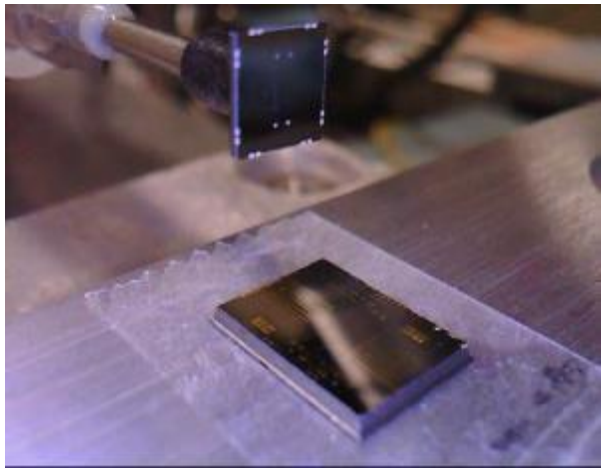
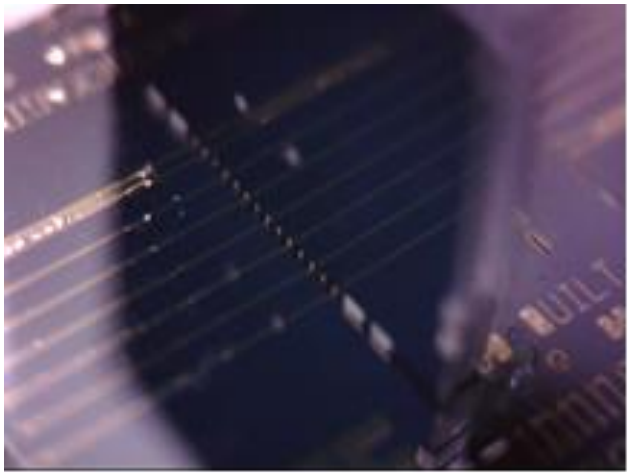
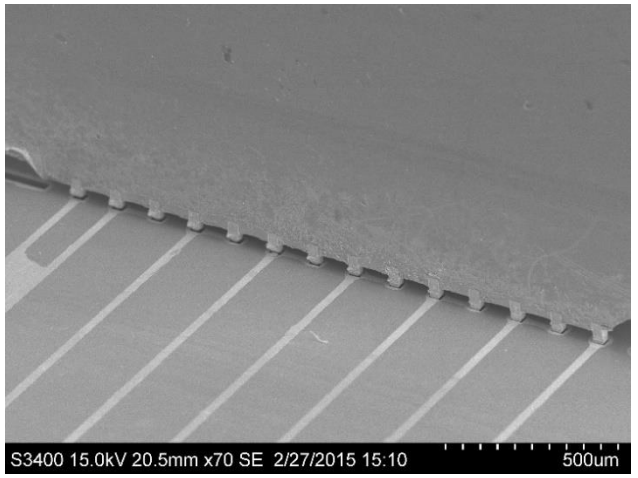
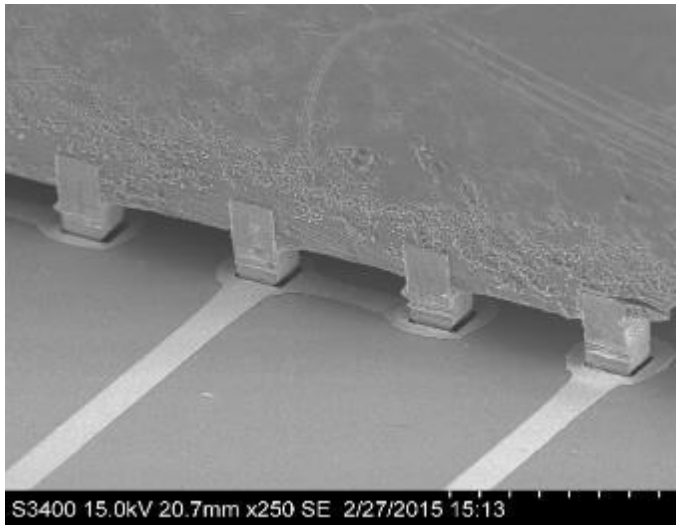
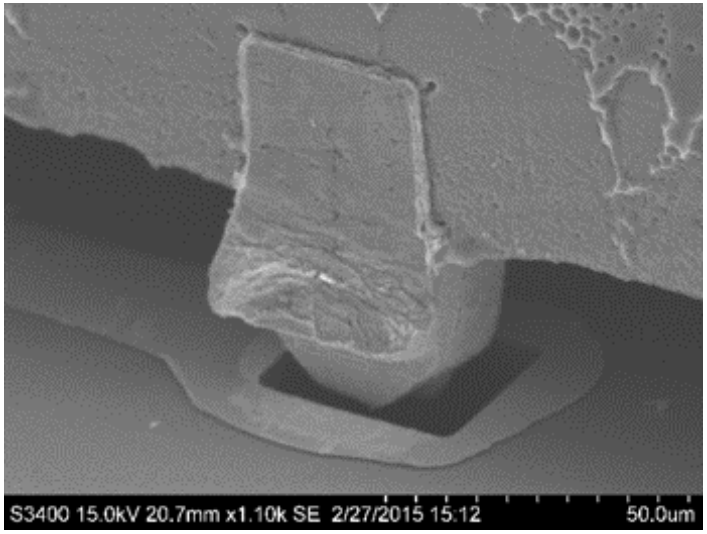
3DQP---Orthogonal Integration Demonstration/Progress

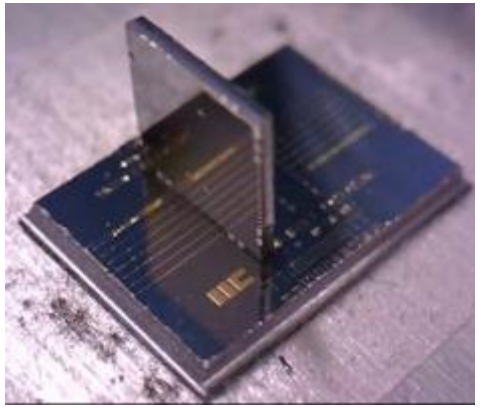












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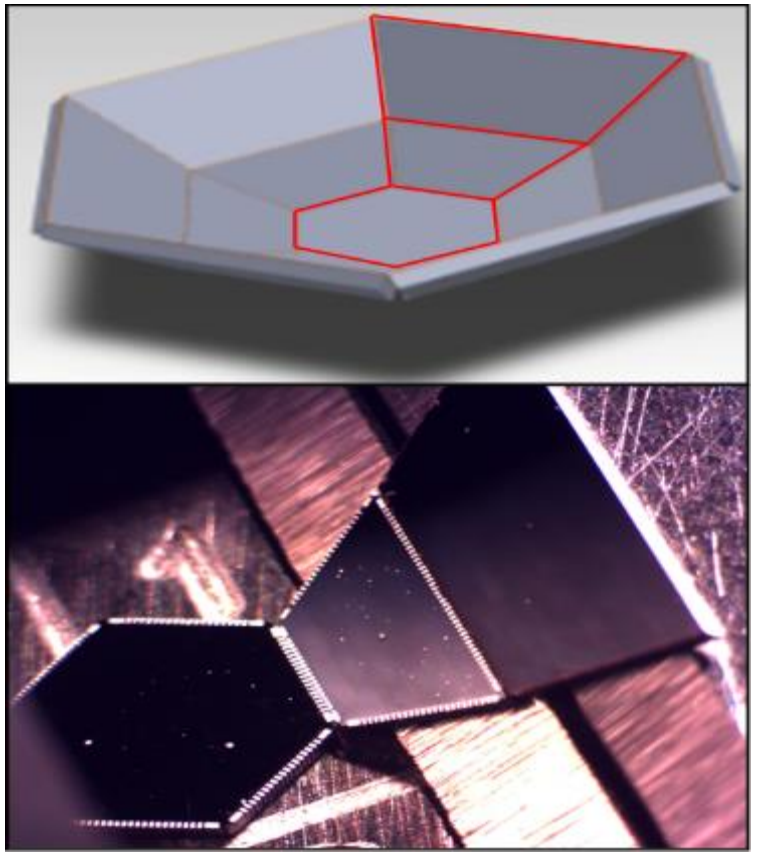
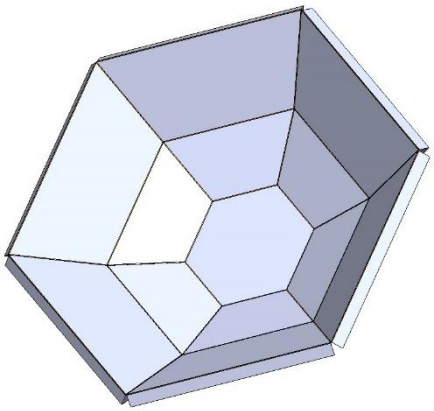
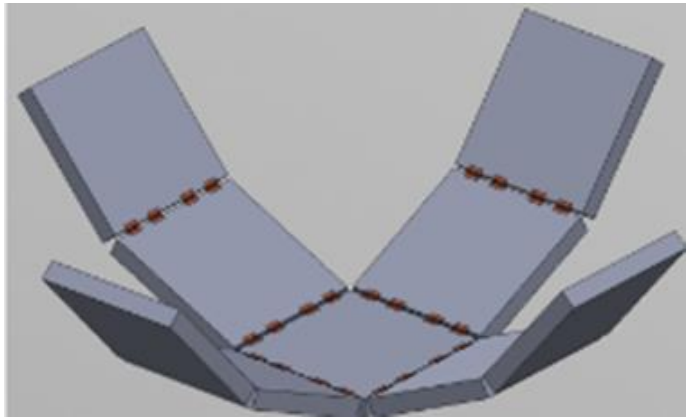
3DQP---Alternative Geometries

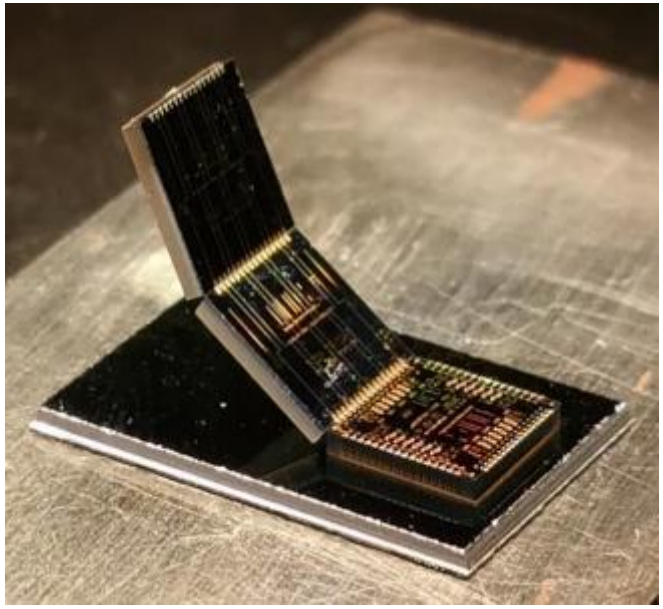
- Unique chip shapes can be fabricated due to singulation of wafer by etching
- QP interconnect nodules enable multiple approaches for I/O, mechanical strength and angle variation
- Application primarily for curved imaging arrays and conformal structures
- Technology demonstration currently underway

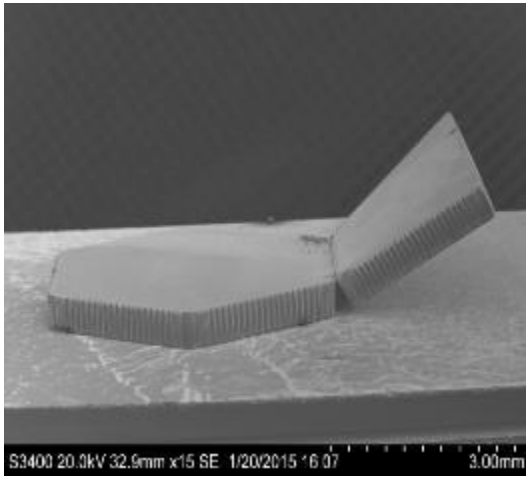


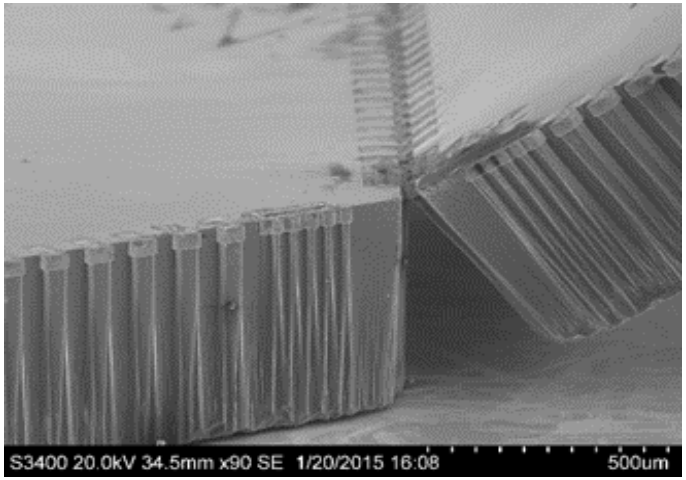
3DQP Alternative Geometries Demonstration/Progress











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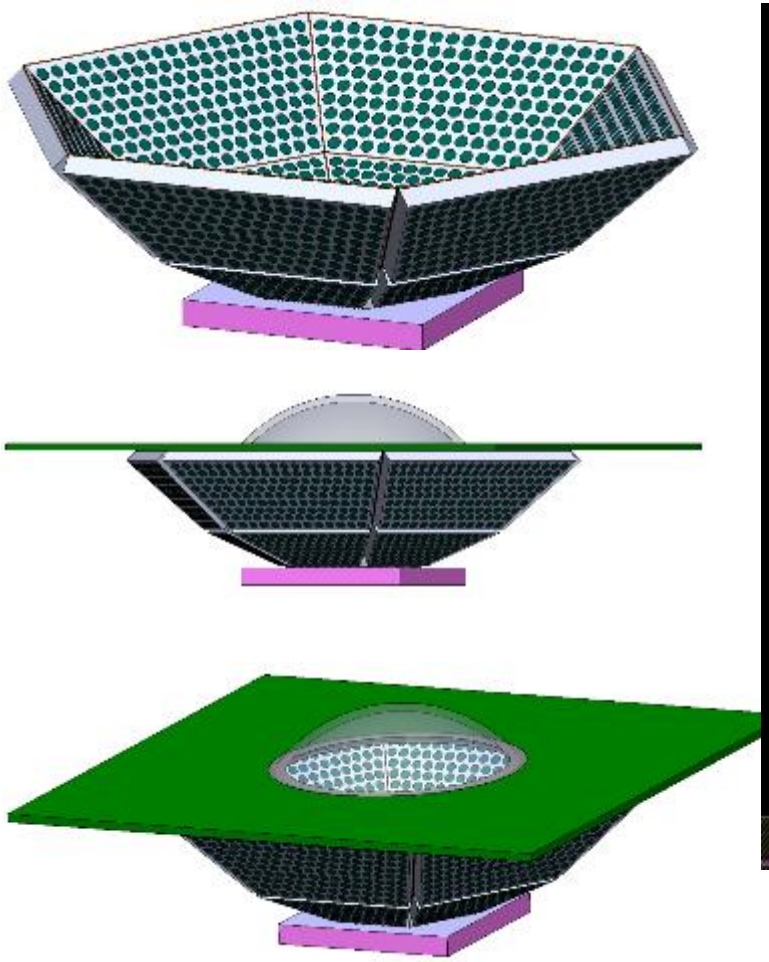
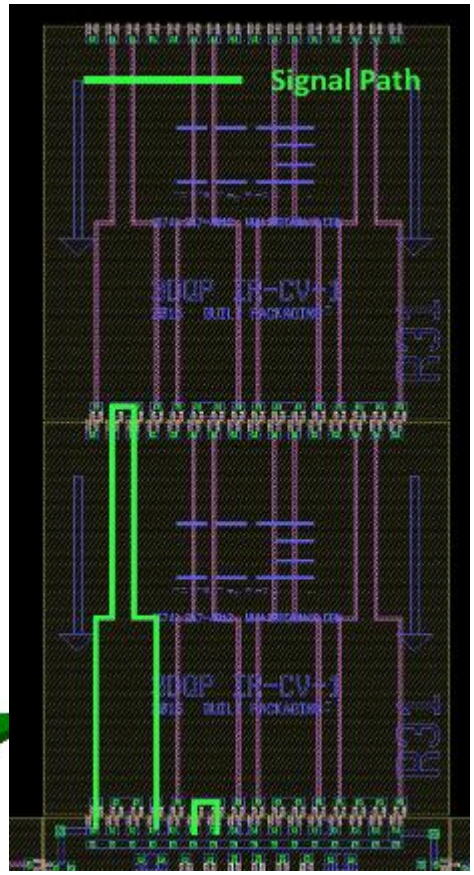
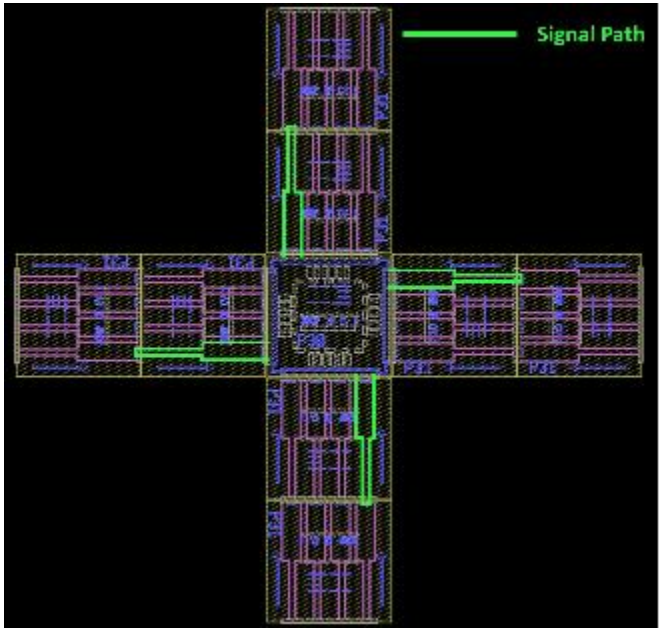
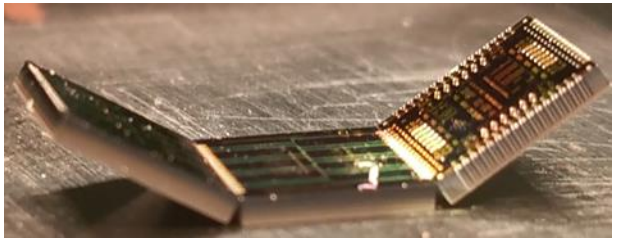
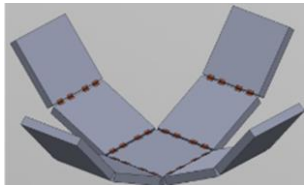
3DQP Alternative Geometries Electrical Test Demonstrator











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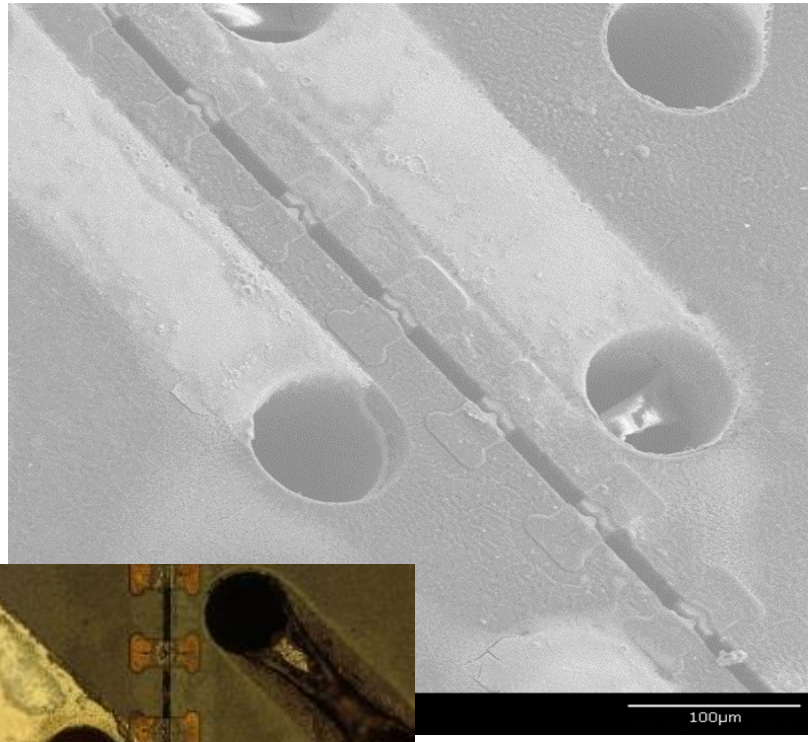
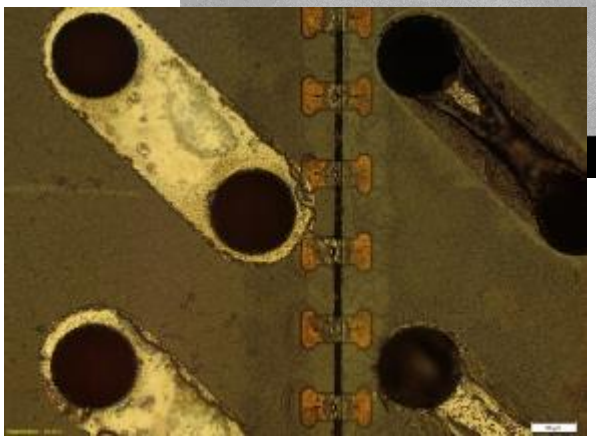
3DQP---QP + Stacking

- Integration of QP with TSV (barrel & filled vias)
- QP interconnect nodule requires very little keep-out area from vias
- “Best of All Worlds” approach decreases tradeoffs
- Applications include large format arrays, system minaturization





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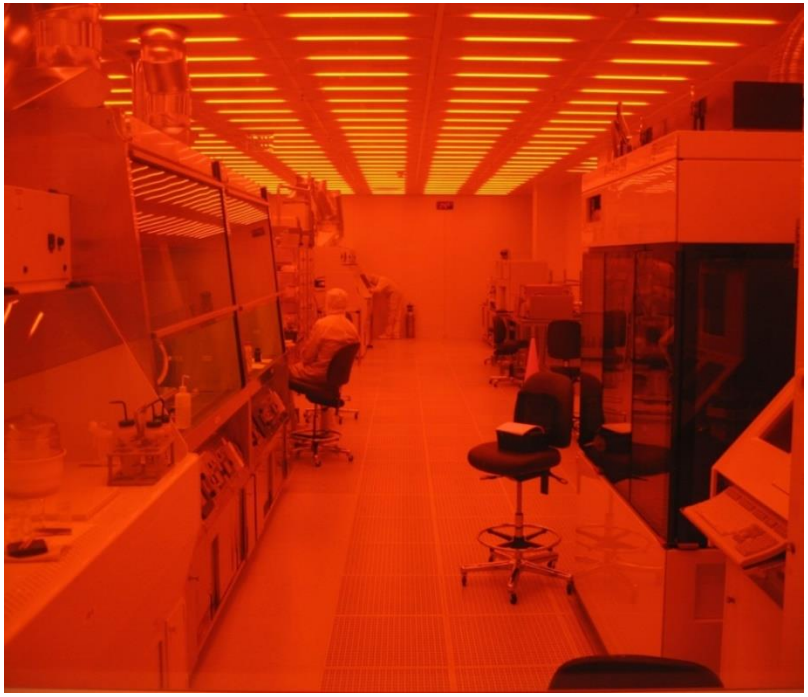
Summary of Quilt Packaging Benefits

- Optimized integration of disparate materials and process technologies (Si, GaAs, GaN, SiGe, AlN, more)
- Enables new 3D system architectures beyond just stacking
- Chip partitioning for optimal yield/functionality
- Sub-micron chip-to-chip alignment (FPAs, IRSPs, Optical)
- Better thermal management due to all chips on heatsink
- Reduced power dissipation, die size, design cycle time
- Variety of interconnect geometries & sizes available simultaneously
- Increased IP flexibility, security & design re-use
- Complementary with existing packaging approaches---can be combined w/TSV, WB, bumping, etc.

Thank You!

- IIC works with customers or collaborators on specific applications of QP technology
  - RF/microwave
  - Power Electronics
  - Optical & optoelectronics
  - High Performance Computing
  - MEMs integration in 3D
- Mechanisms for Collaboration
  - Development Engineering for QP
  - Joint proposals
  - Contract R&D



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